LDPC Encoder/Decoder v1.0

PB052 March 3, 2022 **LogiCORE IP Product Brief**

Introduction

The Low Density Parity Check (LDPC) soft IP core supports LDPC decoding and encoding. The LDPC codes used are highly configurable, and the specific code used can be specified on a codeword-by-codeword basis.

Additional Documentation

A product guide is available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/ldpc-enc-dec.html

Features

- LDPC decode or encode of a range of customer specified Quasi-cyclic (QC) codes
- Throughput(1) up to:
  - 1.77 Gb/s for LDPC decode @ 8 iterations
  - 12.4 Gb/s for LDPC encode
- High bandwidth AXI4-Stream interfaces

1. See performance in the Product Guide for clock frequency of 400 MHz. Throughput depends on the codes and how they are mixed and the actual clock frequency on the device.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale™, UltraScale+™, Virtex-7, Kintex-7
Supported User Interfaces	AXI4-Lite, AXI4-Stream
Provided with Core	
Design Files	N/A
Example Design	IP Integrator Block Diagram
Test Bench	Verilog
Constraints File	Xilinx Design Constraints (XDC)
Simulation Model	System Verilog Secure model Bit-accurate C model MEX file for use with MATLAB
Supported S/W Driver	Standalone
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

Forward Error Correction (FEC) codes such as Low Density Parity Check (LDPC) codes provide a means to control errors in data transmissions over unreliable or noisy communication channels. The LDPC Encoder/Decoder core provides an optimized block for encoding and soft-decision decoding of these codes. Custom and standardized LDPC codes are supported through the ability to specify the parity check matrix through an AXI4-Lite bus. A block diagram of the LDPC Encoder/Decoder core is shown in Figure 1.

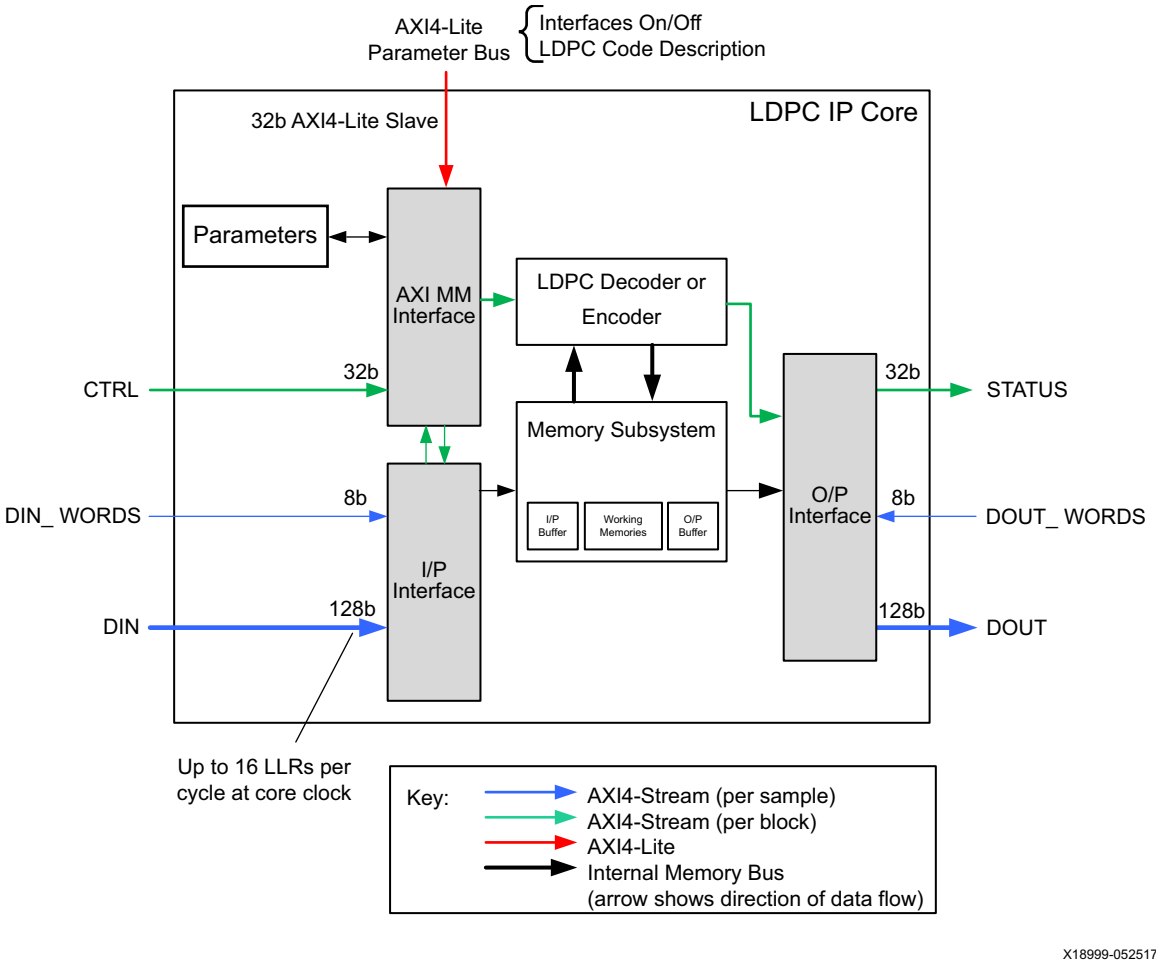

Figure 1: **LDPC Encoder/Decoder Core Block Diagram**

Feature Summary

The LDPC Encoder/Decoder core is a highly flexible soft-decision LDPC decoder and encoder with the following features:

- Highly configurable codes
  - A range of quasi-cyclic codes can be configured over an AXI4-Lite interface
  - Code parameter memory can be shared across up to 128 codes
  - Codes can be selected on a block-by-block basis
- Normalized min-sum decoding algorithm
  - Normalization factor programmable (from 0.0625 to 1 in steps of 0.0625) for layers
- Number of iterations between 1 and 63
  - Specified for each block
- Early termination
  - Specified for each block to be none, one, or both of the following:
    - Parity check passes
    - No change in hard information or parity bits since last iteration
- When configured as a decoder, soft or hard outputs
  - Specified for each block to include information and optional parity
  - 6-bit soft Log Likelihood Ratio (LLR) input and 8-bit output (8-bit interface, 2 fractional bits, with external saturation before input to symmetric range -7.75 to +7.75 assumed)
- In- or out-of-order execution of blocks, with user specified ID field to identify blocks
- Interfaces
  - Wide data interfaces on input and output
  - Ability to specify number of LLR values on either a block-by-block basis or transfer basis
  - Separate inputs to specify control parameters and receive status output on a block-by-block basis

Applications

The LDPC Encoder/Decoder core is intended for use in applications requiring LDPC encode/decode, such as 5G wireless, backhaul, and DOCSIS 3.1 cable modems.

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

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Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
03/03/2022	1.0	Removed Export Control Disclaimer. It is not required for this document.
10/04/2017	1.0	Initial Xilinx release.

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